SLG8SP585

Clock Synthesizer for Intel PCI-Express Gen2 Chipset

Features

- SLG8SP585 is fully compliant to Intel CK505 clock specification revision 1.0
- SRC clocks compliant to PCI-Express Gen2 reference clock requirement
- Integrated series terminated resistor
- Scalable I/O : CPU & SRC Output
- 3.3V and low voltage (0.8V) I/O Power Supply
- 32 pin QFN package (Mobile Application)
- ROHS 6/6 Compliant Package
- HF- Halogen Free

Output Summary

- 2 - differential CPU clock outputs @ 0.8V
- 1 - differential DOT96 clock output @ 0.8V
- 1 - single-ended 27MHz clock output @3.3V
- 1 - single-ended 27MHz SS clock output @3.3V
- 1 - differential Selectable SRC/SATA clock outputs @0.8V
- 1- differential Serial Reference Clock (SRC) clock outputs @ 0.8V
- 1 - single-ended 14.318MHz clock output @ 3.3V

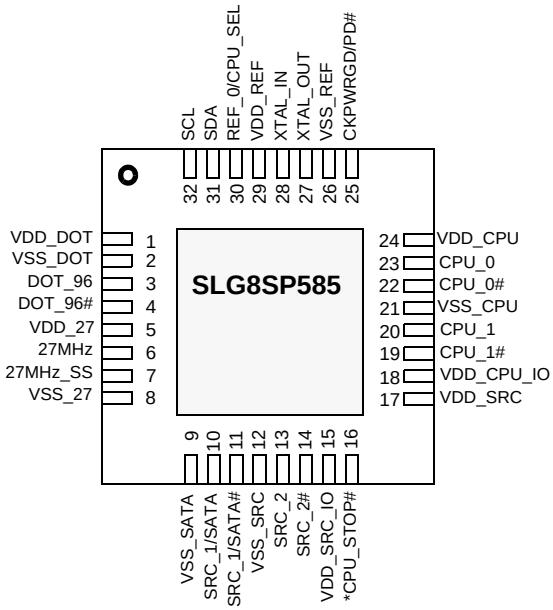
Table 1. CPU_SEL During CK_PWRGD Latch Pin 30

Input (pin 30)	CPU_0	CPU_1
0	133MHz	133MHz
1	100MHz	100MHz

Note: 10K Ohm external pull up or pull down resistor required on CPU_SEL

Table 2. Number of Clock Outputs

Output	Number Output
133MHz	2
SRC(100MHz_SS)	1
SRC/SATA (100MHz)	1
REF (14.3181MHz)	1
DOT_CLK (96MHz)	1
27MHz	1
27MHz SS	1



32-pin QFN
0.50mm pitch
5x5mm
*contains internal pull-up resistor

Pin Description

Pin #	Name	Type	Description
1	VDD_DOT	PWR	3.3V power supply for outputs.
2	VSS_DOT	GND	Ground for outputs.
3	DOT_96	O, DIF	96 MHz DOT clock output.
4	DOT_96#	O, DIF	96 MHz DOT clock output.
5	VDD_27	PWR	3.3V power supply for outputs.
6	27MHz	O, DIF	27MHz non SS Clock Output.
7	27MHz_SS	O, DIF	27MHz SS Clock Output.
8	VSS_27	GND	Ground for outputs.
9	VSS_SATA	GND	Ground for outputs.
10	SRC_1/SATA	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
11	SRC_1/SATA#	O, DIF	Configurable Serial Reference clock for SATA or PCI Express device.
12	VSS_SRC	GND	Ground for outputs.
13	SRC_2	O, DIF	Differential Serial Reference Clock output.
14	SRC_2#	O, DIF	Differential Serial Reference Clock output.
15	VDD_SRC_IO	PWR	Low voltage I/O power supply for outputs.
16	CPU_STOP#	I	3.3V LVTTL input for CPU_STOP#. Contains internal pull-up resistor.
17	VDD_SRC	PWR	3.3V power supply for outputs.
18	VDD_CPU_IO	PWR	Low voltage I/O power supply for outputs.
19	CPU_1#	O, DIF	Differential CPU Clock output.
20	CPU_1	O, DIF	Differential CPU Clock output.
21	VSS_CPU	GND	Ground for outputs.
22	CPU_0#	O, DIF	Differential CPU Clock output.
23	CPU_0	O, DIF	Differential CPU Clock output.
24	VDD_CPU	PWR	3.3V power supply for outputs.
25	CKPWRGD/PD#	I	CKPWRGD is a 3.3V LVTTL iput. It acts as a level sensitive strobe to latch the MODE_SEL and BCLK_SEL pins and other multiplexed inputs. After CKPWRGD assertion, it becomes a real time input for asserting power down (active high).
26	VSS_REF	GND	Ground for outputs.
27	XTAL_OUT	O, SE	14.318MHz crystal output.
28	XTAL_IN	I	14.318MHz crystal input.
29	VDD_REF	PWR	3.3V power supply for outputs.
30	REF_0/CPU_SEL	I/O, SE	14.318 reference clock output. CPU_SEL input.
31	SDA	I/O, SE	Serial Interface bus data input and output.
32	SCL	I	Serial Interface bus clock input.

Block Diagram

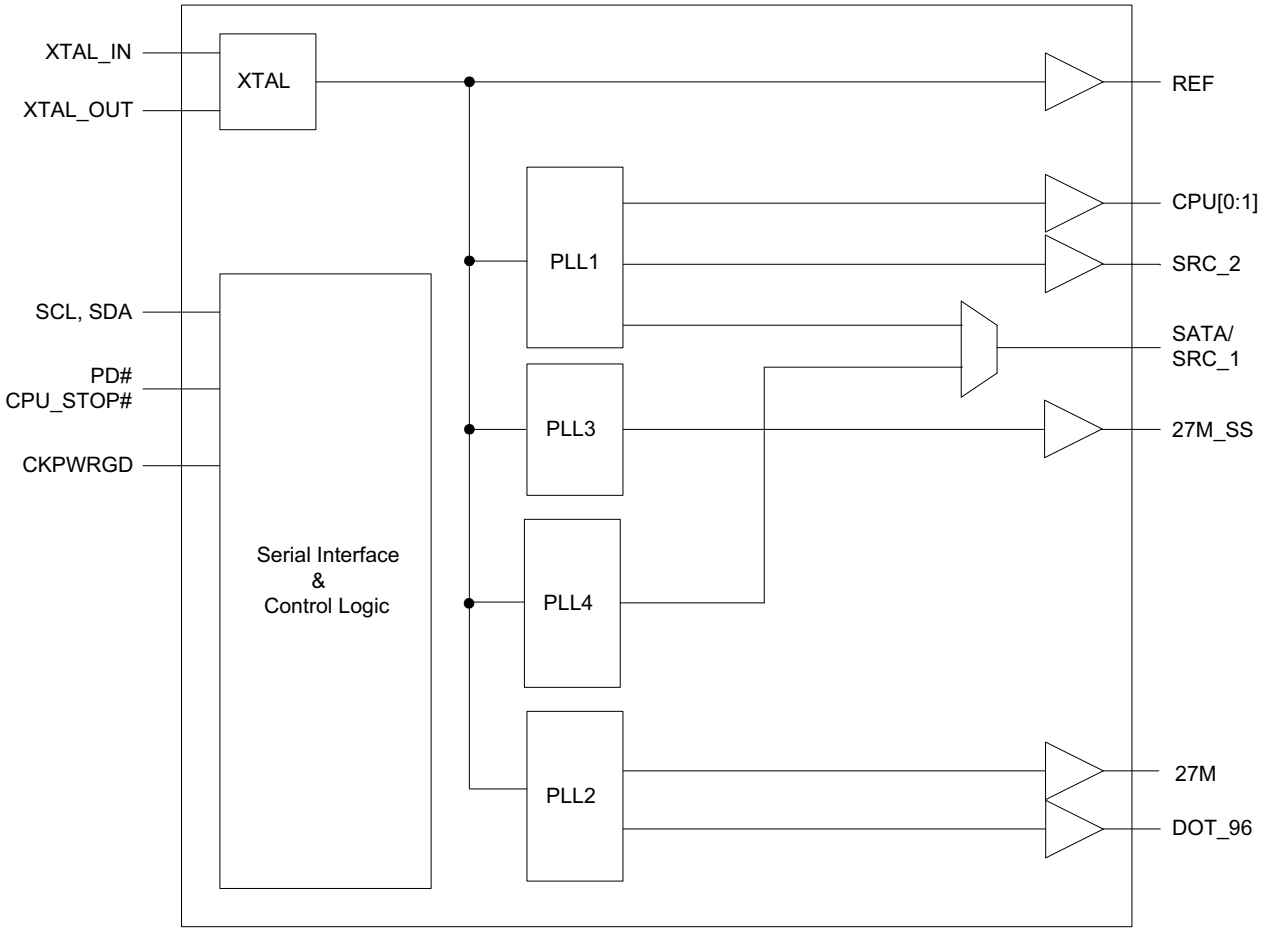


Figure 1. Simple Block Diagram

Enhanced Scalable VDD type “SR” differential output buffer for mobile application

The CK505 utilizes a new output buffer for all differential clocks. The low power type SR buffer is a departure from the type X buffer used in previous CK410 clock generators. The Silego enhanced SR buffer uses custom drivers powered off from a scalable voltage power supply ranging from 1.05V to 3.3V, offering reduction in implementation cost and power consumption. It also improves edge rate performance, and cross point voltage control. In addition, the Silego enhanced SR buffer integrates the 33 ohm series termination resistors, which simplifies board layout and eliminates 20 passive components.

Low Voltage VDD_I/O Implementation Note (VDD_I/O = 1.05V)

The scalable VDD_I/O architecture in the SLG8SP585 is designed to accommodate a variety of low power mobile configurations. One such example is when the clock chip VDDIO is sourced from very low voltages such as 1.05V. Designed this way, significant power savings can be realized.

The CK505 Clock Synthesizer Specification already anticipates and allows for aggressive low power implementations. When using the SLG8SP585 with VDDIO=1.05V, some rounding of the waveform top edges are expected to occur. Because of variation in trace length and loading, the resulting slew rate can be somewhat affected. The SLG8SP585 has additional compensation available for those applications. Design engineers can set Control Register 9, Bits 2:0 to ‘111’ if additional slew rate is desired.

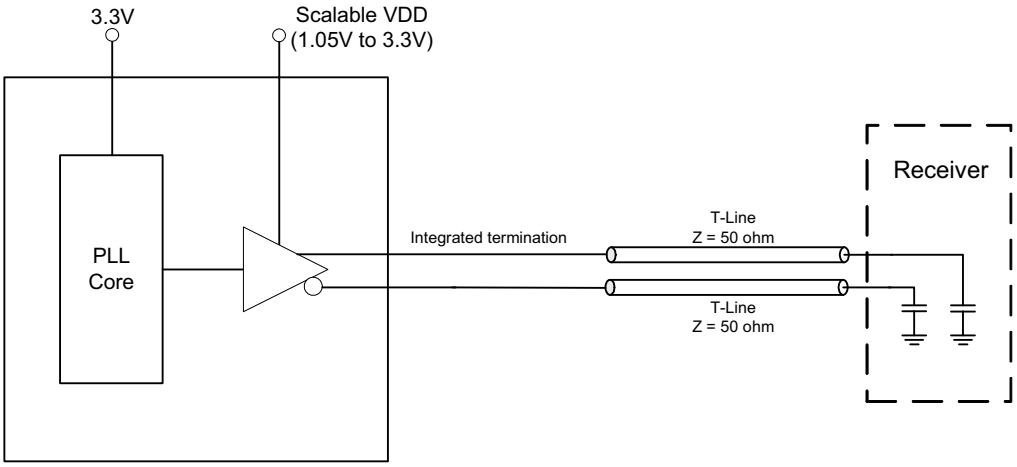


Figure 2. Type SR Differential Output Buffer

Silego CK505 with Integrated Linear Regulator

The SLG8SP585 eliminates the need of external pass element such as a common 2N3904 (SOT23) NPN transistor or a BSS138 MOSFET. The highly integrated CK505 drivers from Silego supports SR type output buffers with a scalable VDD_I/O power supply ranging from 1.05V to 3.3V. It simplifies layout, reduce implementation cost and BOM cost.

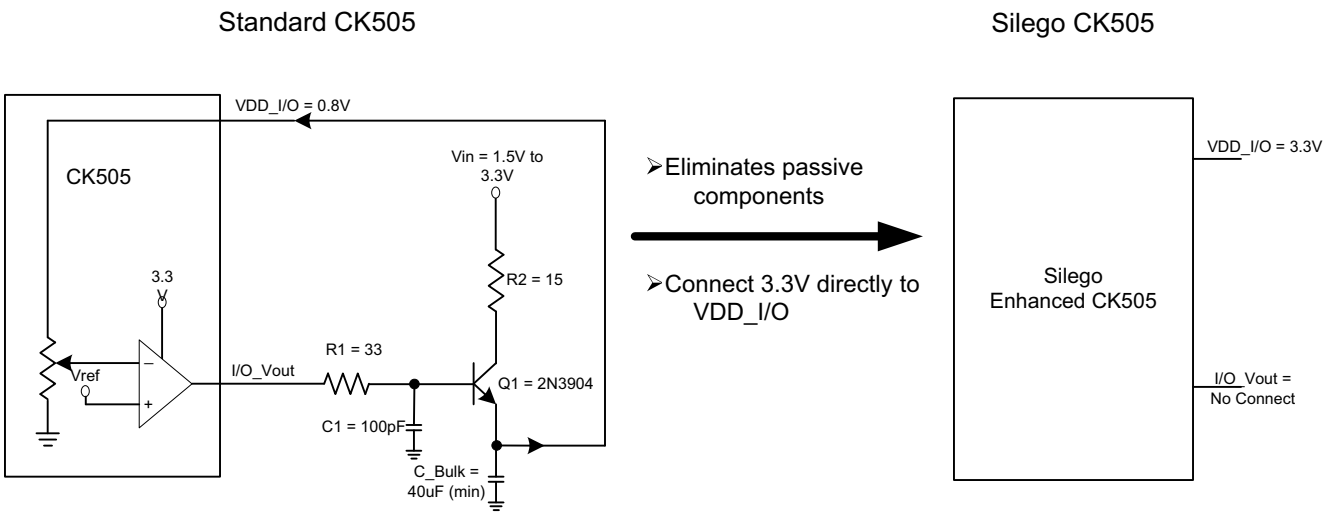


Figure 3. Silego CK505 with Integrated Linear Regulator

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 3*. The slave receiver address is 11010010 (D2h).

Table 3. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Register Summary

Control Register 0

Bit	Type	Description/Function	Power up condition
7	RW	CPU_SEL 0 = 133MHz 1 = 100MHz	*latched status of CPU_SEL*
6	R	Reserved	0
5	R	Reserved	1
4	RW	iAMT Enable 0 = Legacy Mode 1 = iAMT Mode Note: Once this bit is set, it cannot be disabled or cleared by writing a “0”. This bit can only be cleared by a power-on-reset.	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	SRC_1/SATA select 0 = SRC_1 (-0.5% downspread) 1 = SATA (non-SS)	0
0	RW	Configuration control for power down mode 0 = Upon assertion of PD#, the clock generator will initiate a full reset. Under this condition, the clock generator will emulate a cold power on reset internally and re-latch the FS input pins 1 = Legacy PD# input mode	1

Control Register 1

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	PLL1 (CPU PLL) center spread enable 0 = down spread 1 = center spread	0
5	RW	Reserved	0
4	RW	Reserved	0
3:1	RW	27M_SS spread spectrum magnitude control 000 = Reserved 001 = Reserved 010 = 0.5% 011 = 1.0% 100 = 1.5% 101 = 2.0% 110 = 2.5% 111 = Reserved	010
0	RW	Reserved	1

Control Register 2

Bit	Type	Description/Function	Power up condition
7	RW	REF Output Enabled 0 = Disabled 1 = Enabled	1

Control Register 2 (continued)

Bit	Type	Description/Function	Power up condition
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	Reserved	1
3	RW	Reserved	1
2	RW	Reserved	1
1	RW	Reserved	1
0	RW	Reserved	1

Control Register 3

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	Reserved	1
5	RW	Reserved	1
4	RW	Reserved	1
3	RW	Reserved	1
2	RW	Reserved	1
1	RW	Reserved	1
0	RW	Reserved	1

Control Register 4

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	1
6	RW	SRC_1/SATA Output Enabled 0 = Disabled 1 = Enabled	1
5	RW	SRC_2 Output Enabled 0 = Disabled 1 = Enabled	1
4	RW	DOT_96 Output Enabled 0 = Disabled 1 = Enabled	1
3	RW	CPU_1 Output Enabled 0 = Disabled 1 = Enabled	1
2	RW	CPU_0 Output Enabled 0 = Disabled 1 = Enabled	1
1	RW	PLL1 (CPU PLL) Spread Spectrum enable 0 = Disabled 1 = Enabled	1
0	RW	27MHz_SS Spread Spectrum enable 0 = Disabled 1 = Enabled	1

Control Register 5

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 6

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	RW	Reserved	0
5	RW	Reserved	0
4	RW	Reserved	0
3	RW	Reserved	0
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 7

Bit	Type	Description/Function	Power up condition
7	R	Revision ID bit 3	0
6	R	Revision ID bit 2	0
5	R	Revision ID bit 1	0
4	R	Revision ID bit 0	0
3	R	Vendor ID bit 3	0
2	R	Vendor ID bit 2	1
1	R	Vendor ID bit 1	1
0	R	Vendor ID bit 0	0

Control Register 8

Bit	Type	Description/Function	Power up condition
7:4	R	Reserved	0001
3	RW	Reserved	1
2	RW	Reserved	1
1	RW	27MHz output enable 0 = Disabled 1 = Enabled	1

Control Register 8 (continued)

Bit	Type	Description/Function	Power up condition
0	RW	27MHz_SS output enable 0 = Disabled 1 = Enabled	1

Control Register 9

Bit	Type	Description/Function	Power up condition
7	RW	Reserved	0
6	R	Reserved	X
5	RW	REF_0 output slew rate control. Please refer to Control Register 13 bit 7. 0 = 1x (2 loads) 1 = 2x (3 loads)	1
4	RW	REF or Tristate Select for Test Mode 0 = Tristate 1 = REF	0
3	RW	Test Clock Mode Entry Control 0 = Normal operation 1 = REF or Tristate mode Note: If Byte 0 Bit 1 = 1, SATA output remains at 100MHz during test mode enable	0
2:0	RW	IO_VOUT control 000 = 0.3V 001 = 0.4V 010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V 110 = 0.9V 111 = 1.0V	101

Control Register 10

Bit	Type	Description/Function	Power up condition
7	R	Reserved	1
6:2	RW	Reserved	00000
1	RW	Allow control of CPU_1 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1
0	RW	Allow control of CPU_0 with assertion of CPU_STOP# 0 = Free Running 1 = Stopped with CPU_STOP# asserted	1

Control Register 11

Bit	Type	Description/Function	Power up condition
7:1	RW	Reserved	0000000
0	RW	Reserved	1

Control Register 12

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	00
5:0	RW	Byte count register for block read operation Note: The default value is 13. To read more than 13 bytes, system BIOS needs to change this register to the number of bytes it intends to read.	001101

Control Register 13 (Manufacturing Test Control)

Bit	Type	Description/Function	Power up condition
7	RW	REF_0 slew rate control with Control Register 9 bit 5. (B13b7, B9b5) 00 = 1.0V/ns 01 = 1.3V/ns 10 = 1.6V/ns 11 = 2.0V/ns Normal mode default is ‘11’ WF mode default is ‘01’	1
6	RW	Reserved	0
5:4	RW	27MHz slew rate control 00 = 1.0V/ns 01 = 1.3V/ns 10 = 1.6V/ns 11 = 2.0V/ns Normal mode default is ‘10’ WF mode default is ‘01’	10
3:2	RW	27MHz_SS slew rate control 00 = 1.0V/ns 01 = 1.3V/ns 10 = 1.6V/ns 11 = 2.0V/ns Normal mode default is ‘10’ WF mode default is ‘01’	10
1	RW	Individual output slew rate control bit. 0 = Disable 1 = Enable	0
0	RW	Wireless Friendly (WF) mode Enable 0 = Disable 1 = Enable	0

Control Register 14 (Reserved)

Bit	Type	Description/Function	Power up condition
7	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	0
6:0	RW	Reserved	XXXXXX

Control Register 15 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Control Register 16 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Control Register 17

Bit	Type	Description/Function	Power up condition
7:6	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	00
5:3	RW	Reserved	000
2	RW	Reserved	0
1	RW	Reserved	0
0	RW	Reserved	0

Control Register 18 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	00000110

Control Register 19

Bit	Type	Description/Function	Power up condition
7:1	RW	Reserved	0000000
0	RW	Vendor Manufacturing/Production Test Mode. Please write with “0”	0

Control Register 20

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	10
5:4	RW	Reserved	10
3:2	RW	Reserved’	10
1:0	RW	Reserved	10

Control Register 21

Bit	Type	Description/Function	Power up condition
7:6	RW	Reserved	10
5:2	RW	Reserved	1010
1:0	RW	Reserved	10

Control Register 22 to 28 (Reserved)

Bit	Type	Description/Function	Power up condition
7:0	RW	Reserved	X

Crystal Recommendations

The SLG8SP585 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG8SP585 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 5. Crystal Recommendations.

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Cut Accuracy (max.)	Temp Stability (max.)	Aging (max.)
14.31818MHz	AT	Parallel	20pF	0.1mW	5pF	0.016pF	35ppm	30ppm	5ppm

Absolute Maximum Ratings

Max VDD Supply Voltage (VDD_3.3):.....4.6V

Max VDD_I/O Supply Voltage (VDD_I/O):.....4.6V

Max Input Voltage (Vih):.....4.6V

Min Input Voltage (Vil):.....-0.5V

Storage Temperature::..... –65°C to + 150°C

Operating Temperature (Ambient, no airflow): . 0°C to +70°C

ESD Protection (Min):..... 2000V

DC Electrical Characteristics

Operating Conditions

Symbol	Description	Conditions	Min	Typ	Max	Unit
VDD_3.3	3.3V Supply Voltage	±5%	3.135		3.465	V
Vih	Input High Voltage (SE) for MODE_SEL		2.4		VDD+0.3	V
Vil	Input Low Voltage (SE) for MODE_SEL		VSS-0.3		0.8	V
Vih_FS_Normal	Input High Voltage (FS) for CPU_SEL		0.7		1.5	V
Vil_FS_Normal	Input Low Voltage (FS) for CPU_SEL		VSS-0.3		0.35	V
Iil	Input Leakage Current	0 < Vin < VDD	-5		+5	uA
Voh	Output High Voltage (SE)	Ioh = -1mA	2.4			V
Vol	Output Low Voltage (SE)	Iol = 1mA			0.4	V
VDD_I/O	Low Voltage Differential I/O Supply Voltage		1.050		3.465	V
Cin	Input Pin Capacitance		1.5		5	pF
Cout	Output Pin Capacitance				6	pF
Lpin	Pin Inductance				7	nH
Idd_3.3V	Operating Supply Current, default configuration				250	mA
Idd_IO_0.8V	Differential I/O current, all output enabled		25		80	mA
Idd_PD_3.3V	Powerdown Supply Current, 3.3V				1.0	mA
Idd_PD_0.8V	Powerdown Supply Current, 0.8V				0.1	mA
Idd_M1_3.3V	M1 Mode Supply Current, 3.3V				25	mA
Idd_M1_0.8V	M1 Mode Supply Current, 0.8V				8.0	mA

AC Electrical Characteristics

Differential Outputs (CPU, SRC, DOT_96) Timing Characteristics

Symbol	Description	Min.	Max.	Unit	Conditions
Laccurracy	Long term accuracy		100	ppm	Using frequency counter with the measurement interval equal or greater than 0.15 second
Tperiod	Average CPU Period (133MHz, SSC disabled)	7.497751	7.502251	ns	Average period over 1 us
Tperiod	Average CPU Period (133MHz, SSC enabled)	7.497751	7.539950	ns	Average period over 1 us
Tperiod	Average DOT_96 Period (96MHz)	10.41354	10.41979	ns	Average period over 1 us
Tabs	Absolute Min/Max CPU Period (133, SSC disabled)	7.412751	7.587251	ns	
Tabs	Absolute Min/Max CPU Period (133, SSC enabled)	7.412751	7.624950	ns	
Tabs	Absolute Min/Max DOT_96 Period (96MHz)	10.16354	10.66979	ns	
Slew_rise	Rising slew rate[1]	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_fall	Falling slew rate[1]	2.5	8.0	V/ns	1. Use 'average' acquisition mode of the scope 2. Measurement taken from differential waveform 3. Slew rate measured through V_swing voltage range centered about differential zero
Slew_var	Slew rate matching		20	%	1. Use 'average' acquisition mode of the scope 2. Measurement taken from single ended waveform 3. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculation
V_swing	Differential output swing	300		mV	Measurement taken from differential waveform
V_cr	Crossing point voltage	300	550	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. Only applies to the differential rising edge (i.e. Clock rising and Clock# falling)
V_cr_dlt	Variation of V_cr		140	mV	1. Measurement taken from single ended waveform 2. V_cross is defined as the voltage where Clock = Clock# 3. V_cross delta is defined as the total variation of all crossing voltages of rising Clock and falling Clock#
Tccjitter	Cycle to Cycle Jitter (CPU)		85	ps	
Tccjitter	Cycle to Cycle Jitter (SRC)		125	ps	
Tccjitter	Cycle to Cycle Jitter (DOT_96)		250	ps	
Tpj_src	SRC Phase Jitter		3.1	ps	RMS Jitter. PCI-SIG Gen 2
Duty Cycle	Duty Cycle	45	55	%	
Tskew	Pin-to-Pin Skew (CPU_0 & CPU_1)		100	ps	
Tskew	Pin-to-Pin Skew (CPU_2)		150	ps	
Tskew	Pin-to-Pin Skew (all SRC outputs)		3	ns	

Note: [1] May require programming IOVOUT when VDD_IO = 1.05V and certain loading conditions.

REF Timing Characteristics

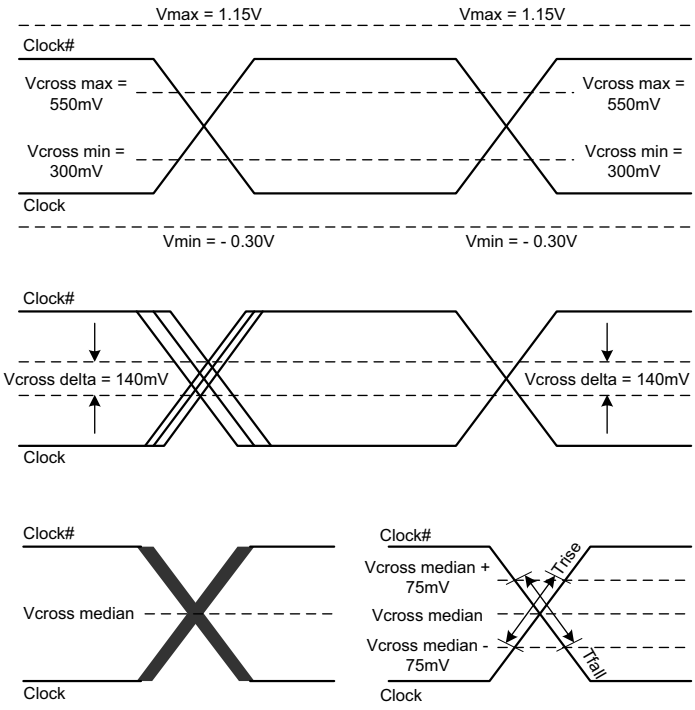
Symbol	Description	Min	Max	Units	Conditions
Laccurracy	Long term accuracy		300	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 14.318180MHz
Tperiod	Average Period	69.82033	69.86224	ns	1. Measured with respect to 1.5V 2. Average period over any 1us period of time
Tabs	Absolute Min/Max Period	68.82033	70.86224	ns	
Thigh	CLK high time	TBD	TBD	ns	
Tlow	CLK low time	TBD	TBD	ns	
Edge Rate	Rising edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Edge Rate	Falling edge rate	1.0	4.0	V/ns	Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system
Tccjitter	Cycle to cycle jitter		1000	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45	55	%	Measured with respect to 1.5V

27M Timing Characteristics (3.3V output)

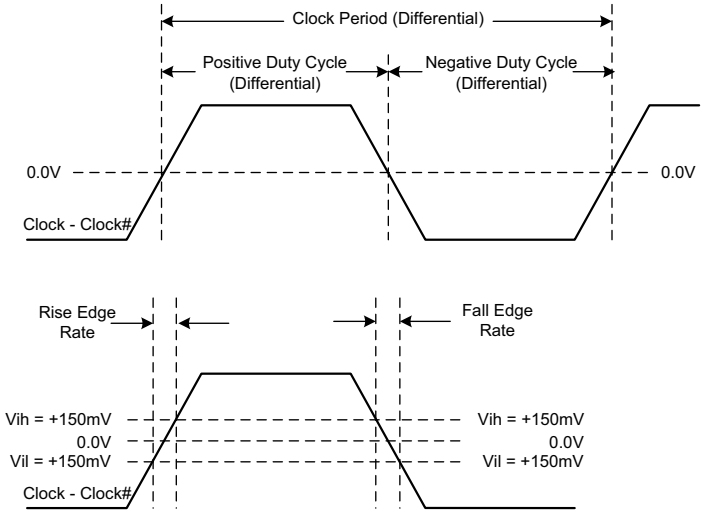
Symbol	Description	Min	Typ	Max	Units	Conditions
Laccurracy	Long term accuracy			±30	ppm	1. Measured with respect to 1.5V 2. Using frequency counter with the measurement interval equal or greater than 0.15s, target frequency is 14.318180MHz
Edge Rate	Rising edge rate	0.5	1	3	V/ns	Measured from 20% to 80% of Vin
Edge Rate	Falling edge rate	0.5	1	3	V/ns	Measured from 80% to 20% of Vin
Tccjitter	Cycle to cycle jitter			200	ps	Measured with respect to 1.5V
Duty Cycle	Duty Cycle	45		55	%	Measured with respect to 1.5V

Measurement Points for Differential Clocks

Single ended (SE) measurement waveforms



Differential (DIFF) measurement waveforms

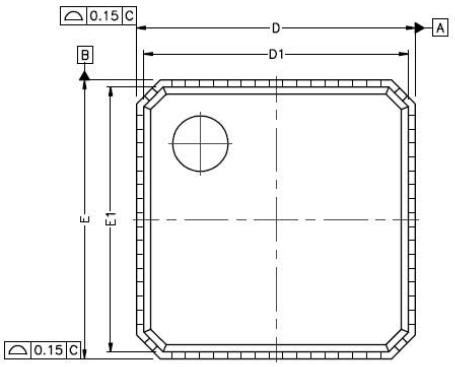


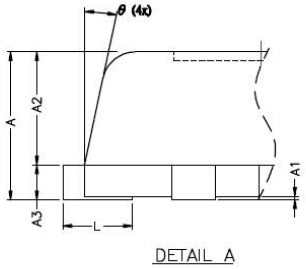
Ordering Information

Part Number	Package Type	Temperature Range
SLG8SP585V	32 Lead Green Package QFN	Commercial, 0° to 70°C
SLG8SP585VTR	32 Lead Green Package QFN - Tape and Reel	Commercial, 0° to 70°C

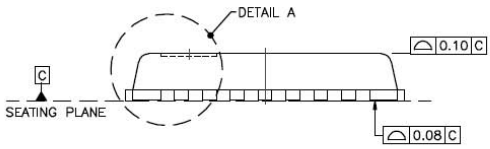
Package Drawing and Dimensions

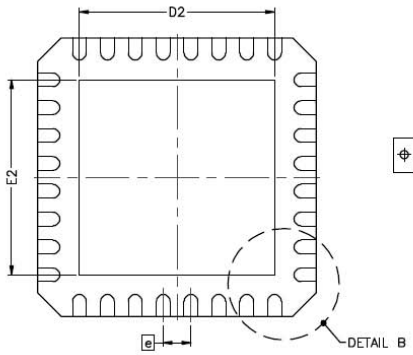
32 Lead QFN Package

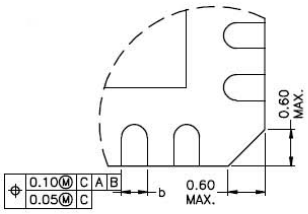




DETAIL A





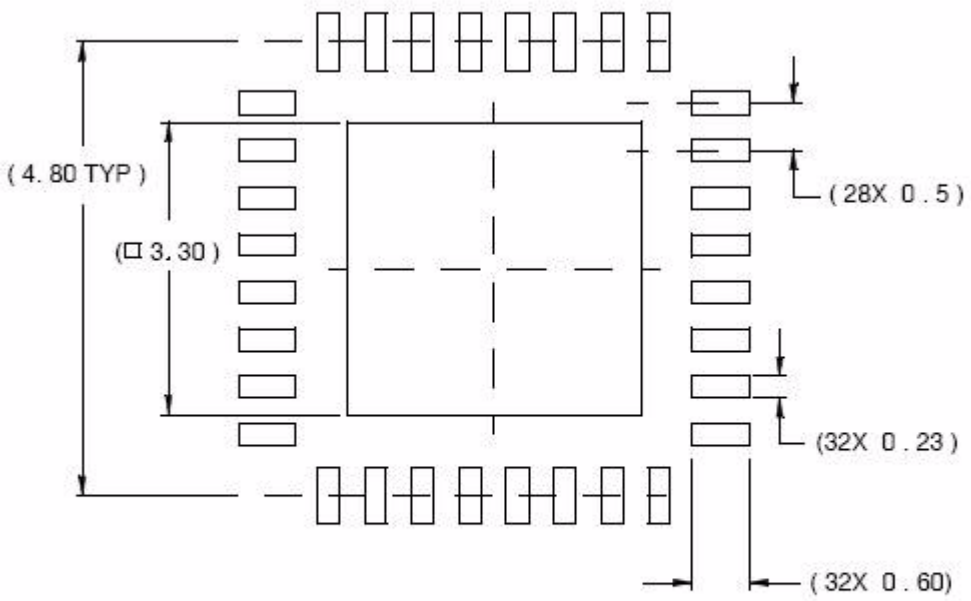


DETAIL B

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	1.00	31	33	39
A1	0.00	0.02	0.05	0	1	2
A2	–	0.65	1.00	–	26	39
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	5.00 BSC			197 BSC		
D1	4.75 BSC			187 BSC		
D2	3.15	3.30	3.45	124	130	136
E	5.00 BSC			197 BSC		
E1	4.75 BSC			187 BSC		
E2	3.15	3.30	3.45	124	130	136
e	0.50 BSC			20 BSC		
L	0.30	0.40	0.50	12	16	20
θ	0°	–	14°	0°	–	14°

NOTE :

1. REFER TO JEDEC STD: MO-220.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.



TYPICAL RECOMMENDED LAND PATTERN